# A NOVEL METHOD TO INCREASE FLUORINE STABILITY TO IMPROVE GAP FILL ABILITY AND REDUCE K VALUE OF FLUORINE SILICATE GLASS (FSG) FILM

## **FIELD OF THE INVENTION**

The present invention relates generally to semiconductor fabrication and more specifically to methods of forming gap-filling films between metal structures.

## **BACKGROUND OF THE INVENTION**

Fluorine silicate glass (FSG) films still suffer from thermal stability issues. The high density plasma chemical vapor deposition (HDP-CVD) deposition rate of FSG films is about 3200 Å/minute which is lower than a CVD deposition of silicon oxide (SiO<sub>2</sub>). The dielectric constant (k) of conventional FSG film is 3.70 and the gap fill for conventional FSG film can only reach  $0.21\mu m$  aspect ratio.

- U.S. Patent No. 6,077,764 to Sugiarto et al. describes an FSG deposition process including an  $N_2$  flow during deposition.
- U.S. Patent No. 6,221,793 B1 to Ngo et al. describes an oxide deposition process including an  $N_2$  flow during deposition.
- U.S. Patent No. 5,827,785 to Bhan et al. describes an FSG process that includes an N-containing gas (NF<sub>3</sub>).
- U.S. Patent No. 5,429,995 to Nishiyama et al. describes a nitrogen and FSG layer.

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 $\mbox{U.S. Patent No. 6,242,338 to Liu et al. describes an $N_2$ plasma} \label{eq:U.S.}$  treatment of an FSG layer.

U.S. Patent No. 6,136,680 to Lai et al. describes various treatments of FSG including a nitrogen-treatment.

U.S. Patent No. 6,103,601 to Lee et al. describes an FSG process and a post treatment.

#### **SUMMARY OF THE INVENTION**

Accordingly, it is an object of one or more embodiments of the present invention to provide an improved method of forming an FSG film.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure is provided. An FSG film is formed over the structure by an HDP-CVD process under the following conditions: no Argon (Ar) - side sputter;  $SiF_4$  flow: from about 53 to 63 sccm; an  $N_2$  flow: from about 25 to 35 sccm; and an RF power to provide a uniform plasma density.

# **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 and 2 schematically illustrate a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Unless otherwise specified, all structures, layers, steps, methods, etc. may be formed or accomplished by conventional steps or methods known in the prior art.

#### Problem Known to the Inventors - Not to be Considered Prior Art

When gaps/openings between metal structures/lines are filling with FSG using conventional HDP-CVD deposition recipes, the corners of the metal structures/lines are clipped off due to sputtering conducted at about a 45° angle.

#### Brief Summary of the HDP-CVD Recipe of the Present Invention

The HDP-CVD recipe of the present invention includes, inter alia:

- 1) nitrogen  $(N_2)$  gas is introduced during the formation of the HDP-CVD FSG to form N-FSG wherein the nitrogen traps free fluorine (F) to prevent the fluorine from diffusing out from the formed N-FSG film;
- 2) a higher SiF<sub>4</sub> flow rate/low bias RF during the HDP-CVD deposition of the N-FSG is used to improve gap fill ability and to eliminate metal structure/line corner clipping; and

3) the RF power is modified to achieve uniform plasma density to achieve deposition of a uniform N-FSG film.

## Initial Structure - Fig. 1

As shown in Fig. 1, a structure 10 includes at least a pair of adjacent structures 12 formed thereover with respective gaps 14 there between.

Structure 10 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Structures 12 are preferably metal structures or lines and are preferably comprised of copper, aluminum or gold and are more preferably copper or aluminum.

The gaps 14 between a pair of adjacent structures 12 are preferably from about 0.19 to  $0.21\mu m$  and may be as narrow as from about 0.17 to  $0.21\mu m$ .

# Formation of N-FSG Film 16 - Fig. 2

As shown in Fig. 2, a nitrogen doped high density plasma chemical vapor deposition (HDP-CVD) fluorine silicate glass (FSG) film 16 (N-FSG) is formed over metal structures/lines 12, filling the respective gaps 14 between adjacent pairs of metal structures/lines 12 in accordance with the recipe of the present invention as describe in detail below.

## HDP-CVD Recipe of the Current Invention

Table I below summarizes the more preferable conditions under which the N-FSG film 16 of the present invention is formed and also lists the conditions of the formation of conventional FSG films for comparison.

TABLE I

Parameter	Conventional	Present Invention
		(all more preferably)
Argon (Ar) - side	50 sccm	0 sccm
Ar - top	5 sccm	about 5 sccm

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SiH <sub>4</sub> flow - side	40 sccm	about 53 sccm
SiH <sub>4</sub> flow - top	3.5 sccm	about 3.0 sccm
O <sub>2</sub> flow	102 sccm	about 138 sccm
SiF <sub>4</sub> flow	30 sccm	about 58 sccm
N <sub>2</sub> flow	0 sccm	about 30 sccm
RF - top power	1500 W	about 1500 W
RF - side power	2 W	about 3400 W
Bias RF power	2500 W	2600 W

It is noted from Table I that in the present invention compared to the conventional process/recipe: the Ar - side is eliminated to decrease the sputter effect and so prevents corner clipping; a greater quantity of  $SiH_4$  - side is employed; a greater flow of  $O_2$  is employed; a greater flow of  $SiF_4$  is employed to increase F etch ability;  $N_2$  is added during the deposition of the N-FSG to trap fluorine to prevent [F] outgassing; and the RF power (RF - top, RF - side and Bias RF) is fine tuned to achieve a uniform plasma density.

The preferably conditions for Table I are:

Ar - side: 0 sccm;

Ar - top: from about 4 to 6 sccm;

SiH<sub>4</sub> flow - side: from about 50 to 56 sccm;

SiH<sub>4</sub> flow - top: from about 2.8 to 3.2 sccm;

O<sub>2</sub> flow: from about 133 to 143 sccm;

SiF<sub>4</sub> flow: from about 53 to 63 sccm;

N<sub>2</sub> flow: from about 25 to 35 sccm;

RF - top: from about 1450 to 1550W;

RF - side: from about 3300 to 3500W; and

bias RF: from about 2575 to 2625 sccm.

Further, the following Table II compares selected characteristics of the convention recipe FSG film to the more preferably characteristics those of the present invention recipe N-FSG film 16:

TABLE II

	k	Gap fill	THK	WIW	D/E	Dep	%F	%F%U
			U%	Range		Rate		
FSG	3.712	0.21µm	1.88%	700Å	2.55	3200Å	4.35%	3.53%
recipe						/min		
N-FSG	about	about	about	about	about	about	about	about
recipe	3.467	0.18µm	1.78%	300Å	2.68	4600Å	7.10%	2.5%
						/min		

a lower F%U%.

where: FSG recipe = convention FSG recipe;

N-FSG recipe = present invention FSG recipe;

THK U% = variation of thickness within a wafer (standard deviation mean)

WIW Range = variation of thickness wafer-to-wafer in a lot

D/E = deposition rate/(etch rate + sputter rate); the index of gap ability

Dep Rate = deposition rate

F% -= % atomic concentration

%F%U = variation of F% concentration within a wafer

The preferably characteristics of the N-FSG film 16 for Table II are:

k: from about 3.3 to 3.5;

gap fill: from about 0.17 to 0.19µm;

THK U%: from about 1.75 to 1.81%;

WIW range: from about 250 to 350Å;

D/E: from about 2.65 to 2.71;

deposition rate: from about 4400 to 4800Å;

%F: from about 6.80 to 7.40%; and

%F%U: from about 2.3 to 2.7%.

It is noted from Table II that the N-FSG film 16 of the present invention as compared to the convention FSG film has: a lower dielectric constant (k) which can reduce line to line (L/L) capacitance about 8%; better gap filling ability (an aspect ratio of about 3.5:1); a lower THK U%; a lower range; a higher D/R; a greater deposition rate (by about 40%); a higher percentage of fluorine; and

Further, the N-FSG film 16 was found to be more stable than the conventional recipe FSG film as to, inter alia: the F%; lack of F outgassing; lack of formation of Si-OH bonds; thermal stability; and high moisture resistance.

The inventors have determined that no Si-OH peak in a Fourier transform infrared spectrum (FTIR) was detected after one week in the N-FSG film 16 formed in accordance with the present invention. Thus, without the presence of Si-OH bonds formed on the N-FSG film 16, water (H<sub>2</sub>O) will not be absorbed by the N-FSG film 16. Also, no bubble after 7 alloys (at about 400°C, N<sub>2</sub>, 45 minute furnace for 7 times – worse case for thermal test) was detected on a patterned wafer employing the N-FSG film 16 of the present invention meaning that fluorine within the N-FSG film 16 was stable and did not outgas, attacking metal structures/lines 14.

As way of example, the inventors have determined the following film quality comparison experimental data between a conventional FSG recipe (SID) film and a present invention FSG recipe film (NFSG):

	SID	<u>NFSG</u>	
Deposition Rate	3194	4348	

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WIW Range	756Å	312Å
[F] Range	0.092	0.073
Dry Etching Rate	5099Å/min	5795Å/min
Dep/Etch Ratio	2.42269188	2.585142857
Total [F]	4.491%	9.943%
Total F%/Film F%	1.080346404	1.373722023
Film Stress	-7.55E+08	-4.61E+08

## Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1.dielectric constant (k) can be reduced from about 3.4 to 3.5 – about an 8% reduction compared to current FSG films;

- 2.high gap-filling capability, can fill down to  $0.17\mu m$  and no need clipping;
- 3.F in N-FSG recipe keeps the film more stable;
- 4. higher deposition rate with improved throughput; and
- 5.the thickness variation for wafer-to-wafer reduced to about 300Å, improved CMP window.

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While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.